NETSPEED SYSTEMS

Product Brief
NetSpeed Orion

NetSpeed Orion: Physically Aware Network-on-Chip IP

Orion is a physically aware, high-performance Network-on-chip (NoC) IP that is used for rapidly designing and analyzing highly efficient and scalable interconnects for a wide variety of SoCs, from mobile to high performance SoCs in enterprise computing and networking. To quickly produce efficient, high-performance NoC IPs, Orion uses a requirements-driven design approach. Orion uses number of state-of-the-art algorithms to provide robust end-to-end QoS and application-level deadlock avoidance. The solution can scale from low- to medium-end SoCs with 10s of IP blocks to high-end SoCs with 100s of IP blocks and provides bandwidth scaling, optimal latency and clock frequencies of up to 3 GHz.

Step 1: Specify

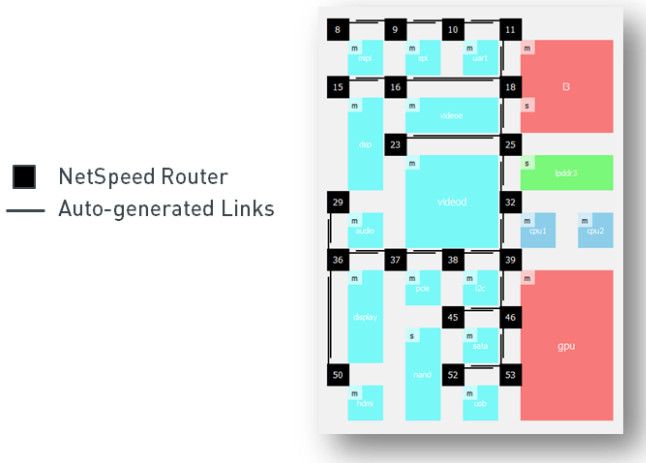
- Components, Connectivity
- PPA Requirements
- SoC Level Use Cases

Step 2: Customize

- Rapid Architectural Exploration
- Real-time Customization
- Power Estimation & Optimization

Step 3: Generate

- Customized On-Chip Network IP



- Synthesizable RTL
- Verification IP
- C++ Functional Models
- PPA Statistics
- Custom Reference Manual

KEY FEATURES

Requirements Driven Approach

Orion offers system architects a better way to design and optimize SoCs. Starting with high-level system requirements as inputs, Orion uses an interconnect synthesis engine to construct an optimized network-on-chip solution. The synthesis engine factors in placement and routing information and automates timing closure.

Physically-Aware Design Flow

Orion design is physically aware of the layout of the on-chip components producing an interconnect topology that is customized for the SoC layout. Being physically aware ensures that wiring congestions does not occur late in the design cycle and appropriate number of buffers and pipeline stages are present at various fabric channels to enable smooth backend design.

Scalable Interconnect Platform

The unique architecture of NetSpeed Orion allows it to **scale performance** to match both the growing number of IP blocks and increasing design complexity. This allows NetSpeed Orion to be used as NoC platform for entire product families.

KEY BENEFITS

Faster Time-to-Market

NetSpeed Orion delivers significant TTM advantages across phases:

- **Architecture**: Rapid floorplan-aware architectural exploration
- **Design**: Automatic resizing of routers, links for optimal PPA
- **Verification**: Correct-by-construction NoC and auto generated testbenches shorten verification cycle
- **ECO**: Algorithmically maintains performance goals while allowing last-minute pipeline additions and other ECO changes

Industry Leading Performance, Power and Area

The fundamental architecture and the underlying hardware elements of NetSpeed Orion are designed for supporting **Tbps on-chip bandwidth and GHz+ operation**. Using these elements, high performance and efficient NoCs can be built for variety of SoCs - from mobile to enterprise networking and high performance computing.

Correct-by-Construction

NetSpeed Orion is constructed to be deadlock free. NetSpeed IP uses graph-theory based approach and formal techniques to ensure that there are no cyclical loops in the entire message dependency chain of the system, thereby ensuring a deadlock-free solution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