Spectral™ Design and Test, Inc.

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MemoryTime™ Product Fact Sheet

Product Overview:

MemoryTime™ provides a comprehensive behavioral model generation, device sizing, design analysis & characterization tool targeted at memory designs and memory compilers. It also addresses the growing needs of memory designers to run statistical analysis, device optimization and characterization of nanometer designs.

Spectral's solution encapsulates standard memory model generation, test benches, bitcell analysis, design margin collection & final design characterization in one concise database. The database can be accessed by users to harvest data or create custom views. MemoryTime automates the process of generating views for industry standard EDA tools.

Key Features:

- Integrated Bitcell analysis engine
- Critical margin collection & analysis
- Timing data collection & analysis
- Power data collection & analysis
- Multithreading job control system
- Handles multiple netlists
- Monte-Carlo analysis support
- Parameterized Verilog Models
- Data verification
- Compiler distribution mode support
- View creation templates
  Verilog, Liberty, Celtic, Primetime
  Datasheets, Functional Testbench

The rich set of features in MemoryTime enables the designers to quickly move thru the various phases of designing complex embedded memories.

Product Description:

MemoryTime™ accepts Spice/Verilog netlists, spice stimulus in industry standard formats. Users specify PVT corners, race conditions in the manner in which they naturally want to run the tool. The different modes supported by MemoryTime™ are Bitcell Analysis, Design Margin & full characterization. The tool creates an ASCII database which can be parsed using interpreted languages like Tcl/Python. The tool can create data-sheets, liberty files, Verilog models and bitcell analysis tables for analysis and 3rd party EDA support. Users can also create custom views using database access utilities and computation capabilities.

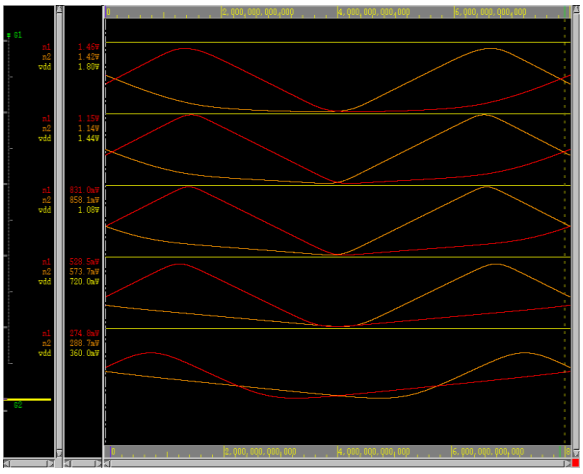

Figure 1
SRAM Bitcell Static Noise Margin (SNM)
at FS Processing, -40C, and Decreasing Voltages

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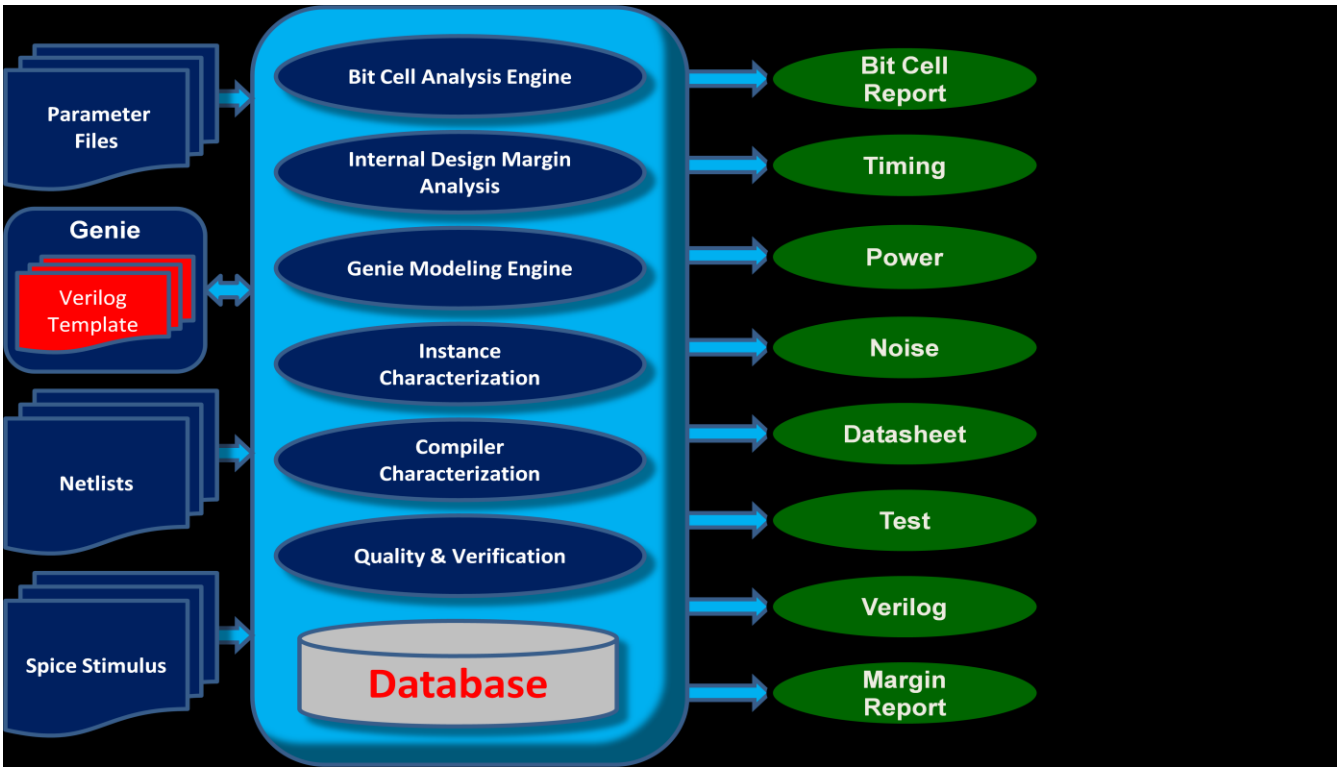

Figure 2: MemoryTime Data Flow

Benefits:

MemoryTime™ benefits circuit designers, device engineers in foundries and memory compiler developers. The tool supports standard spice formats resulting in a fast learning curve. The various steps involved in memory design are effectively captured in a common database. This helps to insure design and data integrity. The job control facility allows designers to make the best use of compute resources. It also works with third party job control systems. MemoryTime's ability to accept multiple netlists and stimulus files enables simulations to be optimized for the particular task. For compilers, once a design is fully characterized a built-in estimator provides fast and accurate timing and power data. MemoryTime also supports a compiler distribution mode.

MemoryTime™ is also ideally suited for producing instance families for complex memories such as embedded Cache or CAMs. Through comprehensive automation of the memory modeling, characterization and data validation process, user's benefit in significant productivity improvement.

About Spectral Design and Test Inc.

Spectral is a Semiconductor Point solution provider targeting systems and semiconductor organizations seeking productivity improvement. Our mission is to solve problems in IC design with an in-house team of domain experts. We offer solutions and specialized services in the fields of Embedded Memory and Design-For-Test.

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