Meridian CDC

Clock Domain Crossing Sign-off Solution

Meridian CDC is the fastest, highest capacity and most precise CDC solution in the market. It performs comprehensive structural and functional analysis to ensure that signals crossing asynchronous clock domains on ASIC, or FPGA devices are received reliably. Meridian CDC is the only solution that enables all aspects of CDC sign-off for 500M+ gate SoC designs.

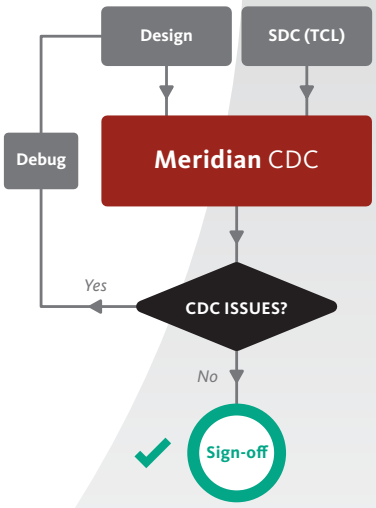
CDC Metastability

CDC bugs are a confluence of bad implementation, clock timing, and digital logic. As shown in Figure 1, if the signal crossing from one asynchronous domain to another arrives too close to the receiving clock edge, the captured value is nondeterministic and leads to signal metastability. These errors are near impossible to detect and diagnose via simulation or in the lab and result in frequent failures in the field that are expensive to fix.

Comprehensive CDC Sign-off

Meridian CDC is the only integrated solution in the industry that combines automatic CDC intent analysis and metastability-aware formal analysis. Meridian CDC's superior technology allows designers to use all of these strategies to guarantee complete CDC correctness. Its flexible top-down and bottom-up hierarchical analysis accommodates the different methodologies used by design teams.

Meridian CDC automatically infers clock domain crossing intent from the design and comprehensively analyzes clock/reset issues, incorrect or missing synchronization, glitch potentials, reconvergence, structurally unsafe crossings and potential data/control crossings that need functional verification. Its comprehensive support of crossing styles and advanced correlation algorithms delivers the fastest and most accurate analysis available.



Meridian CDC's integrated formal analysis exhaustively verifies control and data stability for all data transfer protocols and gray-coding using Real Intent's metastability-aware formal engine. Meridian CDC ensures safe data transfer by verifying the underlying design principle that the CDC data path must be a multi-cycle-path. This goes to the root cause of metastability problems and can be applied to any data transfer protocol.

Meridian CDC's integrated formal solution leverages the automatic CDC intent analysis results to produce a composite report, saving users time and effort. Meridian CDC's integrated formal analysis makes the designer's sign-off task much easier.

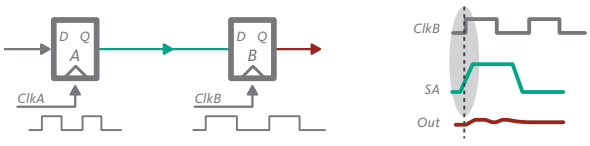


Figure 1. If the signal crossing from one asynchronous domain to another arrives too close to the receiving clock edge, the captured value is nondeterministic.

REAL INTENT

Accelerating RTL Sign-off

Complete HDL Support

Meridian CDC supports the Verilog, VHDL, and System Verilog languages and gate-level netlists. Since RTL logic synthesis performs structural and timing optimizations, which could potentially introduce glitches in the netlist, CDC verification is necessary for both RTL and gate-level netlist representations for complete confidence and sign-off.

Meridian CDC takes advantage of SystemVerilog Assertions (SVA) to guide its analysis and also automatically captures environment information from design files and SDC constraints for easy setup.

Smart Reporting and Powerful GUI

Meridian CDC's smart reporting keeps users focused on important issues through efficient organization of findings. Helpful guidance and suggested actions help users pinpoint the source of the problems quickly. Real Intent's state-of-the-art design intent debugger and analysis manager—iDebug—provides for user configurability and programmability with its command line interface (CLI). All the CDC analysis data is stored in a database that can be accessed through the CLI. So you are not stuck with one methodology that the tool provides for debug. Instead, you can create your own debug methodologies, custom to your own design flows which may include spreadsheet reports, graphical reports, scripting, and so on.

Meridian CDC supports an integrated visualization tool. Pruned schematic views focus on fault-related logic, and with a few mouse clicks, users are directed to the RTL source code that caused the problem. This debug approach allows for easy investigation deep into the design to isolate the root cause for any warnings and errors.

Features

- Automatic design environment capture from designs or SDC constraints
- Comprehensive clock intent inference and analysis catches clock and reset issues
- Metastability aware formal analysis verifies control and data stability
- Flexible top-down and bottom-up analysis to accommodate different design methodologies

Benefits

- Highest capacity to enable CDC verification on 500M+ gate SoC designs
- Fastest performance for quick verification turnaround
- Most precise CDC reporting using integrated analysis
- Easiest-to-use CDC solution in the industry, and is template free
- Multiple technologies to enable complete CDC sign-off from RTL to netlist

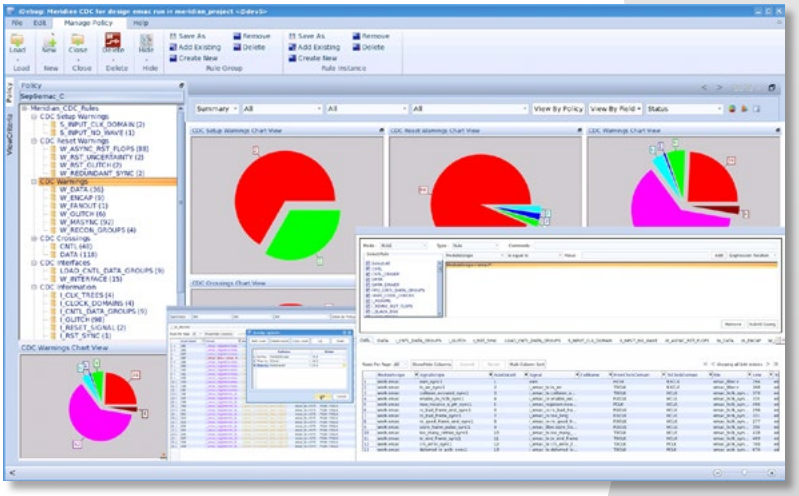


Figure 2. Illustration of customized reporting by Real Intent iDebug for clock domain crossing warnings.

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