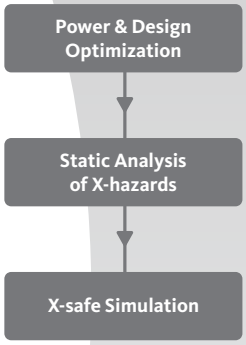
Ascent XV

X-Design and Verification System

The Ascent X-design and verification system (XV) enables the prevention of inaccurate simulation due to X-optimism caused by the propagation of unknowns ('Xs') in RTL designs. XV identifies the X-sources and any X-sensitive constructs, and suggests how to efficiently eliminate X's from uninitialized flops. XV also identifies and corrects inaccurate simulation due to X-pessimism caused by the propagation of unknowns in netlist or gate-level designs. The objective is to eliminate potential issues early in the RTL cycle, and simply detect and correct the issues at the netlist stage. Early sign-off of X issues eliminates costly, painful gate-level debug, and prevents hidden functional bugs from slipping through to silicon.



The Unknown is Dangerous

Design language standards defines an X as an "unknown" when simulation cannot definitely resolve a signal value. Due to simulation semantics, X's can mask bugs in RTL simulation due to X-optimism. While these bugs also show up at the gate level, X-pessimism will cause additional X's. Time consuming iterations between simulation and synthesis are required to debug and resolve differences. Unwarranted X-propagation thus proves costly, causes painful debug, and sometimes allows functional bugs to slip through to silicon. Ascent XV exposes all X-sources at RTL, so you have a complete understanding of where problems might originate.

X-Challenges

Continued increases in SOC integration and the interaction of blocks with various states of power management are exacerbating the X problem. While hardware resets can be used to initialize registers to known values, resetting every flop or latch is not practical because of routing overhead. For synchronous resets, synthesis tools typically clump these with data-path signals, thereby losing the distinction between X-free logic and X-prone logic. This in turn causes unwarranted X-propagation during the reset simulation phase. State-of-the-art low-power designs have additional sources of Xs due to switching between power modes. Ascent XV is a next generation product designed to avoid, detect, and debug X-issues at RTL, and then to correct pessimism in the netlist, ensuring that simulation results will match the hardware behavior.

RTL Static Analysis Reveals X Issues

Ascent XV delivers a comprehensive report for determining how susceptible a design is to the masking of functional bugs due to X-optimism in simulations. All X-sources in the design are automatically identified through structural analysis as well as X-accurate formal reset analysis. The report shows nets in the design that are sensitive to X-optimism due to the propagation of an X from an X-source, and provides debug information with links to the source code and a trace from each net to an X-source in the design.

Reset Optimization

Reset optimization in Ascent XV reduces reset-routing complexity and minimizes power by assessing and then optimizing the number of flops that require hardware resets to ensure a complete initialization. Ascent XV first identifies all X's and then ensures that unknowns are accurately propagated during reset analysis. The report enables analyzing the X-accurate initialization state, and can suggest where to add and/or remove resets to achieve complete initialization.

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Netlist Static Analysis Reveals X-pessimism

Static analysis is also used to identify where pessimism can occur in the design. In the case of pessimism, no changes to the code are advised. Instead side files (SimPortal files) are generated that can be used in the simulation to correct pessimism when it occurs, independent of the test sequence used.

Powerful Debug Interface

Ascent XV comes with a powerful integrated graphical interface. It shows the path from the sensitive construct to an X-source, facilitates waivers of X-Sources and X-sensitive nets, and provides links from source code navigation.

Benefits

- Minimizes susceptibility to simulation inaccuracy due to X-issues that mask functional bugs at RTL and cause unnecessary X's in netlist simulations
- Fast design audit identifies all X-source and X-sensitive constructs that might be driven by an X-source
- Reduces power and routing congestion through optimization and reduction of required hardware resets.
- SimPortal verification automatically generates debug monitors and a simulation free of unnecessary X issues; efficiently identifies and corrects X-pessimism in netlist simulations
- Powerful iDebug graphical debugger with integrated iVision source browser, schematics, and VCDs.
- Correction of pessimism enables the fast bring up of gate level simulations

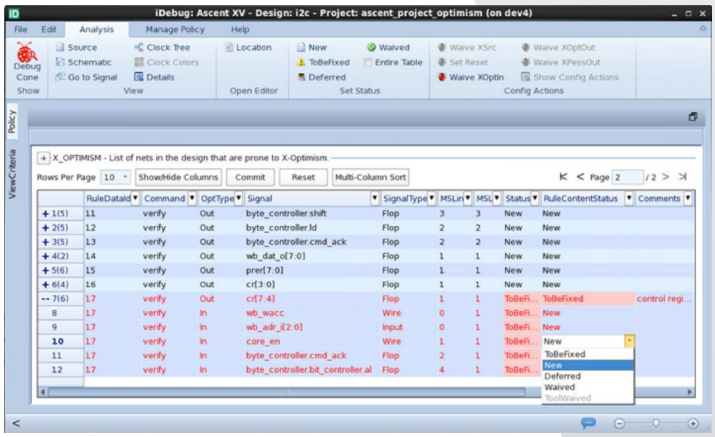

Figure 1. X-optimism analysis highlights X-sources and X-sensitive hardware circuitry.

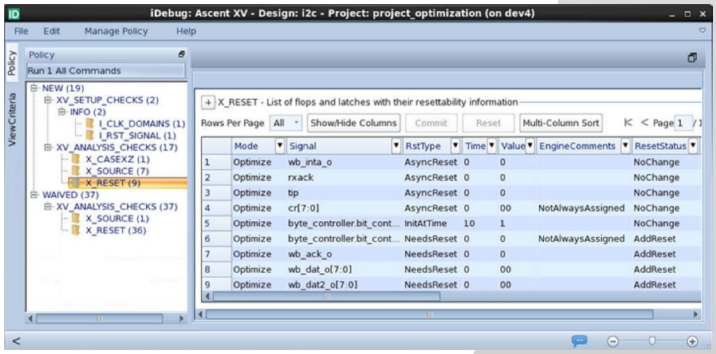

Figure 2. Reset analysis identifies optimization targets.

Real Intent Early Verification Products

Ascent Lint
Automatic RTL Structural Verification

Ascent AutoFormal
Automatic RTL Functional Verification

Ascent XV
X-propagation Management Tool

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