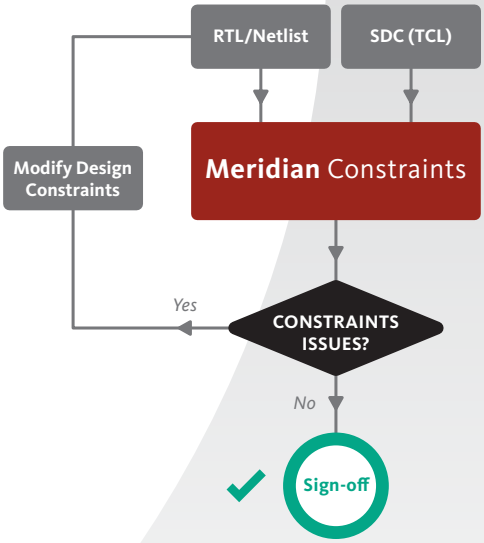
Meridian Constraints

Comprehensive SDC Management and Verification

Meridian Constraints provides, comprehensive design constraint management and verification. It offers high performance constraint validation, template generation, coverage analysis, equivalence checking and timing exception verification capabilities to provide users with the ultimate confidence in the timing constraints employed across all phases of the synthesis and implementation flow.

Timing constraints are used throughout the stages of digital design from synthesis through the implementation flow. At the pre-synthesis stage, timing budgets are established for each design block and then combined to create global constraints for the design. Further adjustment are made to timing constraints, post-synthesis, as the design is technology mapped and actual sign-off timing analysis can be done. After design implementation and routing additional timing data and updated constraints are then realized.Meridian Constraints ensures the correctness, completeness and coverage of these timing constraints (SDC / TCL) as the design moves from RTL to implementation. To ensure completeness of timing constraints, coverage analysis uncovers where definitions are incomplete and features incremental generation capability to extend coverage for the design.

The correct sign-off of timing exceptions minimizes the risk of a re-spin caused by incorrect circuit operation from bad exceptions . The Meridian Constraints functional analysis capability is a unique and powerful way to gain insight into the functionality of your multi-cycle path (MCP) exception control circuitry and how it interacts with exception paths in the design. Based on the latest static engines, this technology is able to validate many types of hardware-controlled multi-cycle paths in a fast and straightforward way. By leveraging functional analysis with the industry-leading formal analysis technology in Meridian Constraints, users have maximum confidence in the correctness of their exceptions.



Meridian Constraints verifies constraints in just minutes and can accelerate clock domain crossing (CDC) verification sign-off by ensuing correct and complete timing data is used. It provides automatic generation of constraints for false paths found in CDC. It is a natural complement to the Real Intent Meridian CDC verification tool.

Easy Adoption

Meridian Constraints is very easy to use. A single script reads in the design and constraint scenarios, either single or multi-mode, and performs all aspects of constraints management. Constraint validation pinpoints syntax, consistency and completeness issues of all design constraints including timing exceptions, which reduces iterations and speeds up higher quality implementation. Reports of violations are based on intelligent checks that reduce the total number to be reviewed and are more meaningful in comparison to other available tools. This makes validation easier and faster for designers.

REAL INTENT

Revolutionary Intent Driven Sign-off

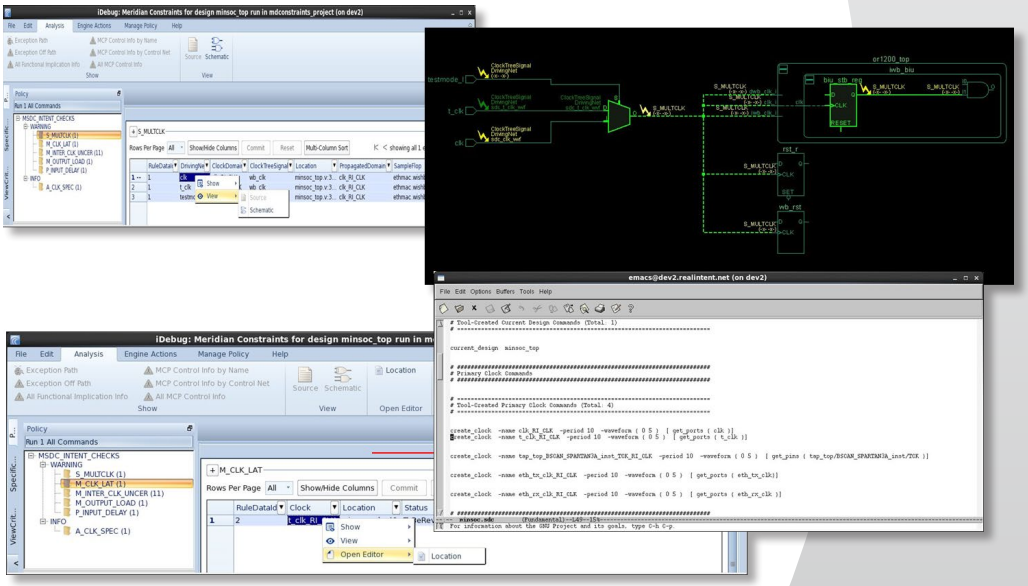
Smart Reporting and Powerful GUI

Meridian Constraints's smart reporting keeps users focused on important issues through efficient organization of findings. Helpful guidance and suggested actions help users pinpoint the source of the problems quickly. Real Intent's state-of-the-art design intent debugger and analysis manager—iDebug—provides for user configurability and programmability with its command line interface (CLI). All the constraint analysis data is stored in a database that can be accessed through the CLI. So you are not stuck with one methodology that the tool provides for debug. Instead, you can create your own debug methodologies, custom to your own design flows which may include spreadsheet reports, graphical reports, scripting, and so on.

Meridian Constraints supports an integrated visualization tool. Pruned schematic views focus on fault-related logic, and with a few mouse clicks, users are directed to the RTL source code that caused the problem. This debug approach allows for easy investigation deep into the design to isolate the root cause for any warnings and errors.

Features

- RTL and gate-level constraint generation
- Incremental constraints template generation from a seed SDC file
- Precise reporting from smart constraints checks
- Fast debugging with cross probing to TCL/SDC, schematic, and design



Smart Reporting makes debug fast and efficient with cross-probing to the RTL design source to pinpoint constraint issues.

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