Meridian Physical CDC

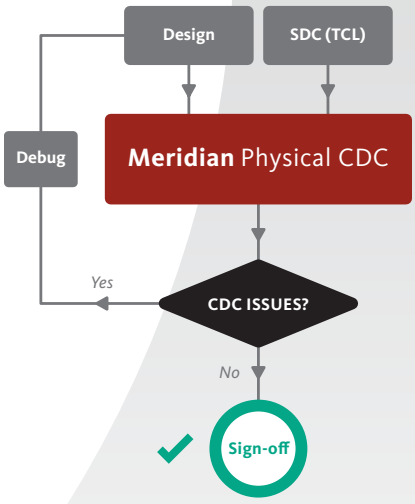
Clock Domain Crossing Sign-off Solution for Gate-level Netlists

Meridian Physical CDC is the only solution available which does complete glitch checking and netlist sign-off. It performs comprehensive structural and functional analysis to ensure that signals crossing asynchronous clock domains on ASIC, or FPGA devices are received reliably at the netlist gate-level. Complementing Real Intent's Meridian CDC solution that provides comprehensive analysis for RTL sign-off, Meridian Physical CDC provides enhanced netlist sign-off for 500M+ gate designs.

RTL and Gate-Level Divergence

CDC verification traditionally has been targeted at RTL sign-off before physical implementation begins. The CDC problems introduced during synthesis along with the addition of test logic and low-power optimizations are risk factors that have not been covered adequately until now. The Meridian Physical CDC software solution extends sign-off to the implementation stage. With the largest flat capacity of any tool in the industry, Meridian Physical CDC provides verification without sacrificing precision. It ensures a glitch-free implementation for all signal crossings, using the widest set of checks and the latest static analysis engines, including new high-performance formal engines. Implementation engineers can be confident the designs handed off to tape-out are free of CDC bugs.

Meridian Physical CDC targets the post-synthesis stage of SoC design at the gate level, where implementation tools can introduce changes that might cause unintended signal glitches and functional failures. It addresses various failures including glitching on control signals, clock networks and data signal paths, and incorrect optimization of clock synchronizer logic.



Typical Implementation Errors

Implementation tools can introduce a number of potential hazards by failing to take CDC into account. Additional registers inserted by test synthesis, for example, can result in glitches on clock lines that can lead to an increased probability of mis-timing issues.

Clock-gating cells inserted by synthesis tools to reduce switching power may also be incompatible with a good CDC strategy. A combinatorial cell such as an AND gate that follows the register intended to pass a clock signal across the boundary to drive the receiving registers is more likely to experience glitches.

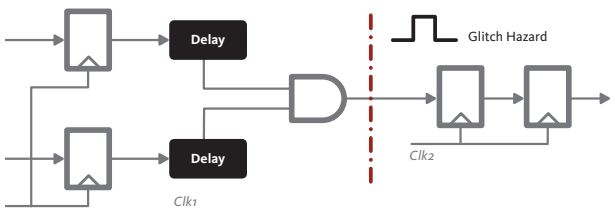


Figure 1. Example Glitch hazard caused by different path delays.

REAL INTENT

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Timing optimization can result in significant changes in logic organization. The optimizer may choose to clone flops so that the path following each flop has a lower capacitance to drive, which should improve performance. If the flops being cloned form part of a synchronizer, this can result in CDC problems. A better way of handling the situation is to synchronize the signal first, and then to duplicate the logic beyond the receiving synchronizer.

The introduction of test logic may even result in the splitting of two flops intended for synchronization. In other situations, optimization of control logic or the use of non-monotonic multiplexer functions can result in the restructuring of CDC interfaces and introduce the potential for glitches.

Smart Reporting and Powerful GUI

Meridian Physical CDC's smart reporting keeps users focused on important issues through efficient organization of findings. Helpful guidance and suggested actions help users pinpoint the source of the problems quickly. Real Intent's state-of-the-art design intent debugger and analysis manager—iDebug—provides for user configurability and programmability with its command line interface (CLI). All the CDC analysis data is stored in a database that can be accessed through the CLI. So you are not stuck with one methodology that the tool provides for debug. Instead, you can create your own debug methodologies, custom to your own design flows which may include spreadsheet reports, graphical reports, scripting, and so on.

Meridian Physical CDC supports an integrated visualization tool. Pruned schematic views focus on fault-related logic, and with a few mouse clicks, users are directed to the RTL source code that caused the problem. This debug approach allows for easy investigation deep into the design to isolate the root cause for any warnings and errors.

Features

- Automatic design environment setup from SDC constraints
- Comprehensively verifies clock, control and data glitches in clock crossings
- Accurate formal analysis using multiple engines
- Option for multi-core runs to reduce runtime significantly
- Easy to debug the crossing glitch issues, includes schematics and waveforms

Benefits

- Most precise CDC glitch reporting using integrated analysis
- Easiest-to-use CDC netlist solution in the industry, and is template free
- Multiple technologies to enable complete glitch-free clock crossing sign-off at netlist

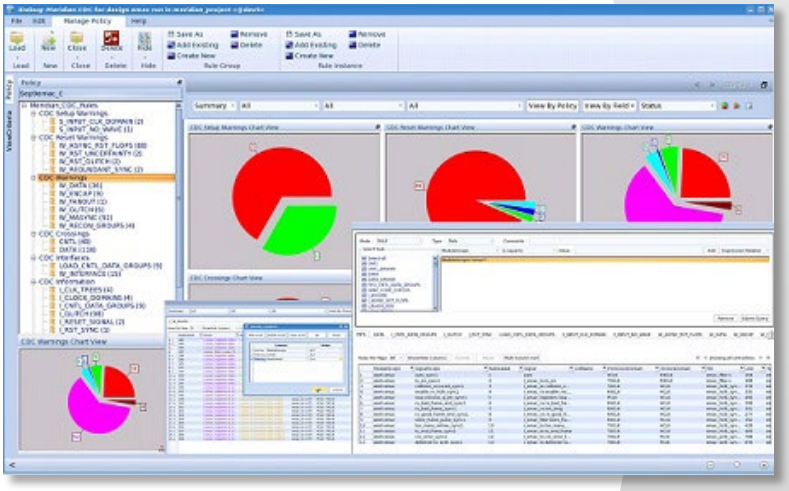

Figure 2. Illustration of customized reporting by Real Intent iDebug for clock domain crossing warnings.

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