VeloceRF™

Inductor, Transformer and Transmission Line
Synthesis & Modeling

Helic®

VeloceRF™ is an inductive device compiler and modeling tool that solves some of your most complex challenges for as low as 10nm geometries.

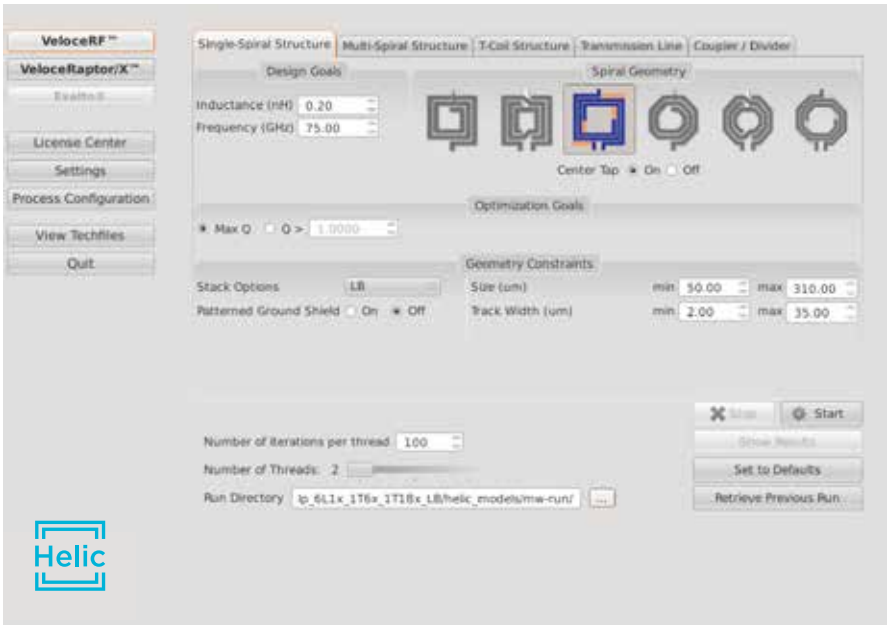
VeloceRF integrates with leading EDA platforms instantiating ready to tapeout layouts and providing highly accurate SPICE models, silicon verified up to 110GHz.

Meet your most exacting inductor needs

VeloceRF shortens the design cycle by greatly reducing the time it takes to synthesize and model complex spiral devices and T-lines. It takes only a few seconds to compile an inductor or transformer geometry and just a couple of minutes to model and analyze it.

With VeloceRF, you can:

- Synthesize DRC/DFM clean devices by design, including metal fill, down to 10nm CMOS.
- Generate passive, causal models in the form of highly compact RLCk netlist models suitable for transient, shooting and noise analyses; and S-parameter models suitable for AC, harmonic balance and SP analyses.
- Get sophisticated PCells/PyCells with maximum flexibility in geometrical parameters (CDFs).

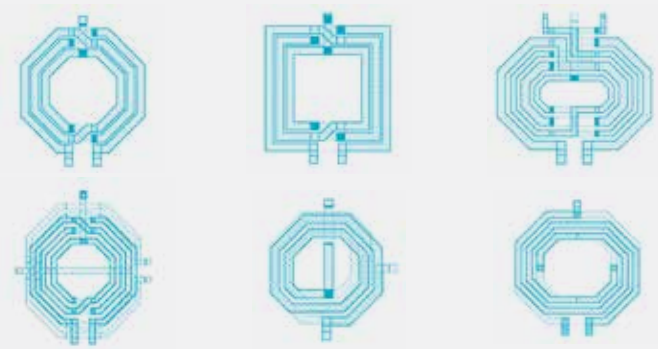


Types of Inductors and T-lines include:

Single-spiral inductors: Differential, single-ended, square and octagonal, with or without center taps.

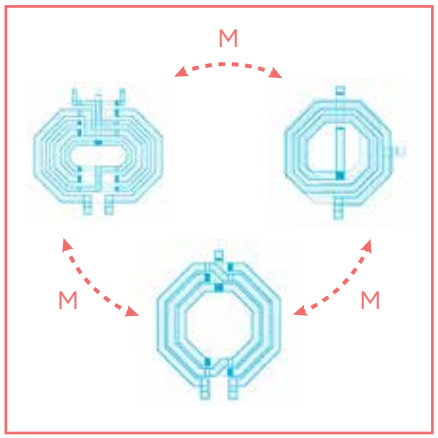
Multi-spiral inductors: Transformers, baluns, T-coils and series differential.

T-lines: Shielded, double-shielded, strip lines, couplers, combiners and other types that are ready to tapeout.



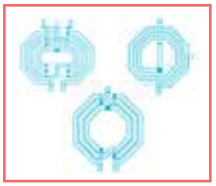
Reduce silicon size - Build perfect floor plan

Inductor size as well as inductor-to-inductor crosstalk can impact the die size.
VeloceRF helps you design smaller devices through the use of optimization criteria and geometry constraints.



In addition, VeloceRF enables you to calculate coupling among any number of inductors to optimize silicon real estate even more.

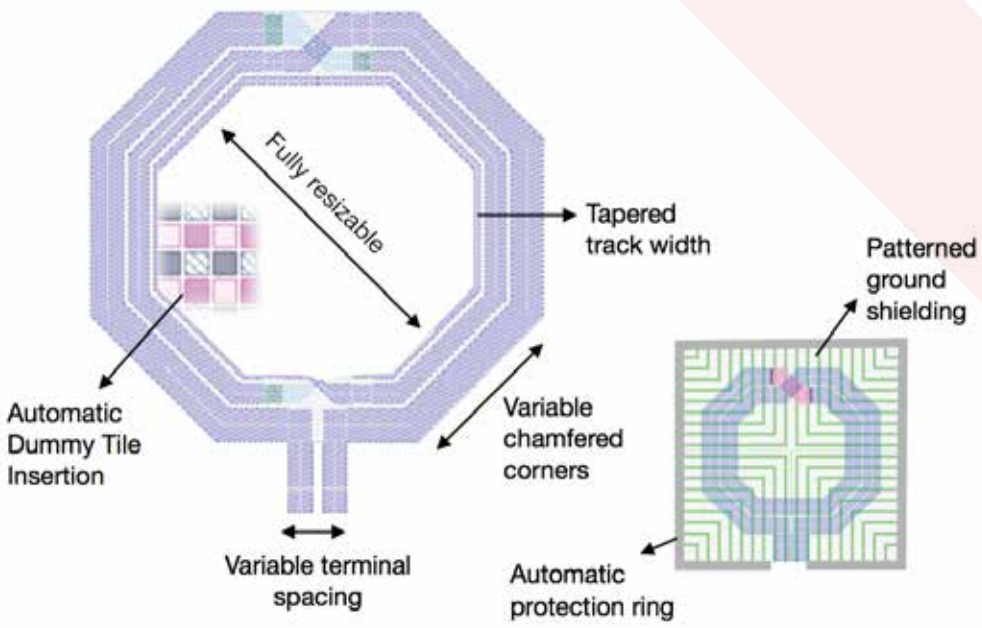
With VeloceRF you can tighten or eliminate guard rings and also optimize the silicon floorplan, taking into account coupling among any number of inductive devices and critical nets, before detailed layout.



Inductor size and EM coupling optimized with VeloceRF

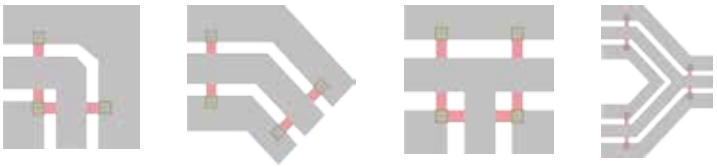
Optimize inductor in circuit context

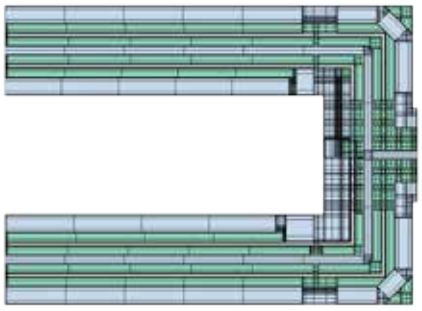
- VeloceRF provides parametric sweep support of inductor parameters to deliver optimal solution in circuit context.
- Mitigates risk in your design by providing silicon proven models accurate up to 110GHz.
- Allows unique coupling analysis among inductors to ensure crosstalk related failures are eliminated.

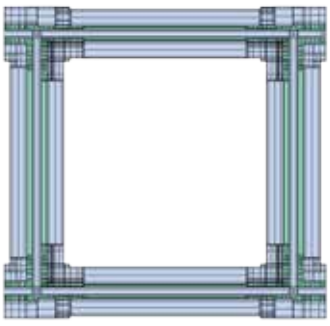


Synthesize millimeter-wave devices for nanometer CMOS in seconds

VeloceRF provides you with proven silicon accuracy to mm-Wave frequencies. A wide array of T-line structures support LEGO-like approach to design including: Microstrip lines, Coplanar Waveguides (Shielded and double-Shielded), Striplines, 45 and 90 degree bends, T-Junctions, Stubs, Branchline Coupler, Wilkinson Divider, etc.







Seamless integration with EDA platforms & foundry design kits

VeloceRF currently supports over 200 unique foundry, process and stack-up flavors. It works with any process including CMOS, BiCMOS, GaAs, SOS and SOI from all semiconductor foundries such as TSMC, UMC, Global Foundries, TowerJazz and Samsung, among others. VeloceRF supports all process nodes down to 10nm.

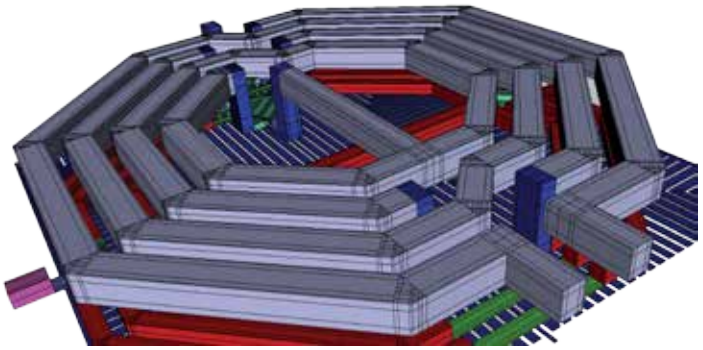
The tool integrates with leading EDA front-end design platforms and with any LVS tool. VeloceRF models can be seamlessly combined with parasitic extracted netlists or views from any parasitics extraction tool.

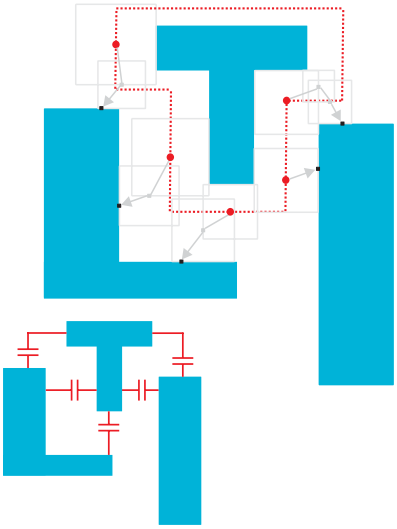
Highest accuracy with Helic's new electromagnetic engine

The RLCk engine that powers the core of VeloceRF pushes the frequency and capacity limits and outperforms any other electromagnetic modeling tool currently available in the market. Helic's RLCk modeling engine comprises the following modules:

Layout Processing

The need to model electromagnetic effects from DC up to mm-wave frequencies calls for special handling of layouts. A novel full 3D meshing algorithm segments the conductors' volume into small cells suitable for accurate modeling of capacitance, inductance and resistance. The engine computes all the Layout Dependent Effects (LDE) before the meshing step.



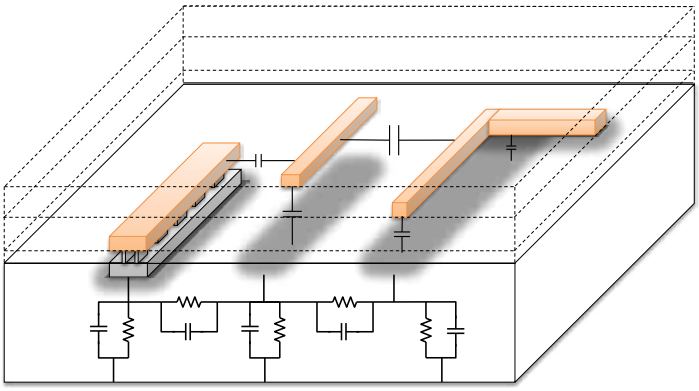


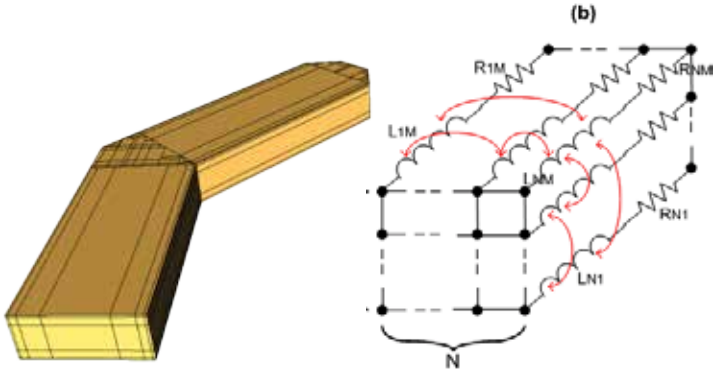
Capacitance Extraction

Helic's 3D capacitance extraction methodology uses a sophisticated stochastic sampling algorithm based on the Random Walk theory for calculating the electric field along the Gaussian surfaces and corresponding coupling capacitances between arbitrary shaped conductors. The solver calculates with the highest accuracy the distributed 3D electric field, using stochastic sampling and a sophisticated numerical solution of the multi-layer Green's function. The method does not use any kind of pattern matching look-up tables or averaging and is free of conductor discretization bottlenecks. It scales way better with circuit size than boundary or volume meshing methods and demonstrates the best computing efficiency since Random Walk is an inherently parallel and extremely fast algorithm.

Substrate Model Extraction

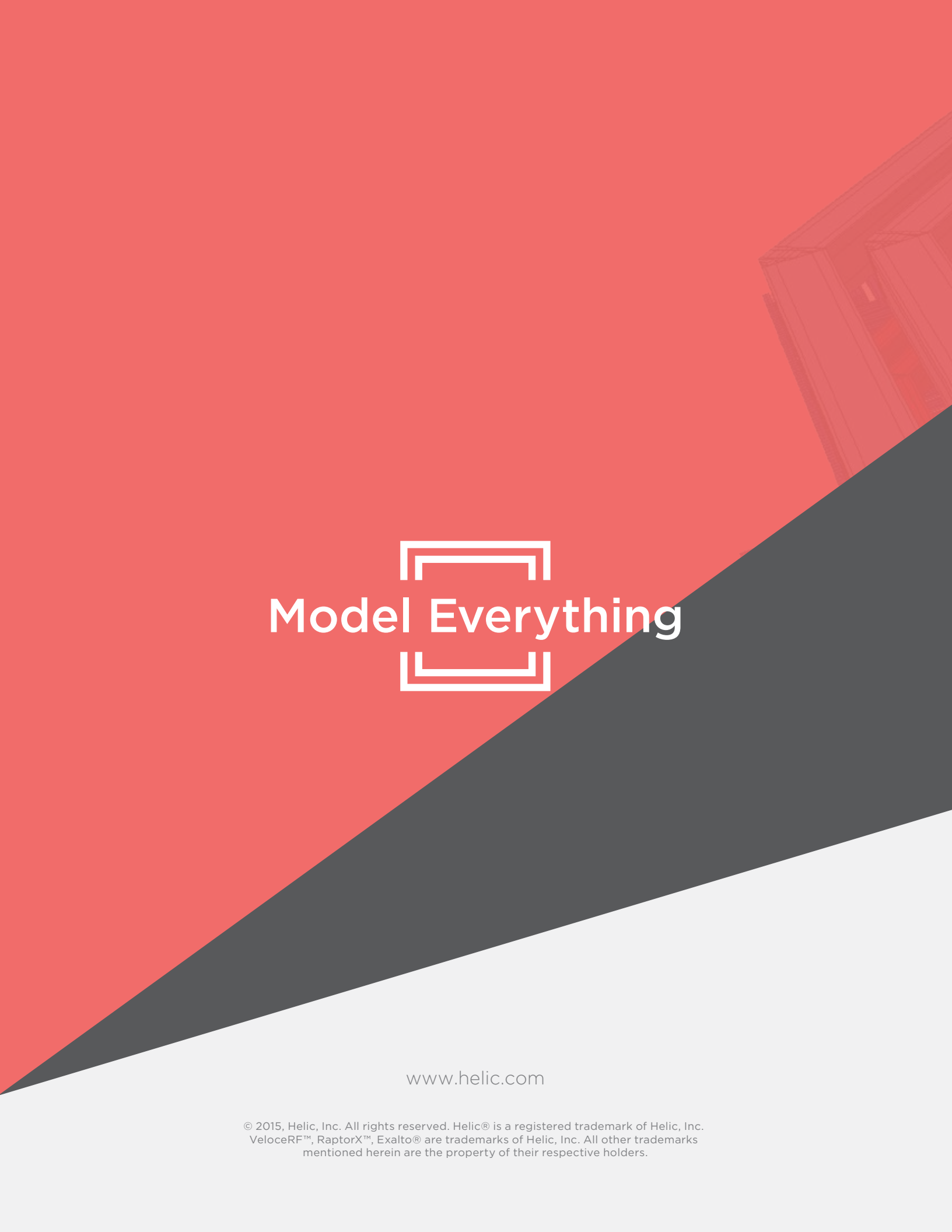
Helic's unique extraction engine models substrate coupling effects with a distributed RC network. A stochastic Monte Carlo based methodology and a 3D substrate model allows for very fast and accurate extraction of the distributed RC substrate network. The method employs a random-walk algorithm that allows characterization of multiple substrate layers using appropriate Green's functions without the need of three-dimensional discretization. The parallel nature of both capacitance and substrate modeling algorithms offers scalability and extraction times superior to any other method.





Inductance and Resistance Modeling

Combines the accuracy of a full-wave electromagnetic (EM) modeling engine with the flexibility and interoperability of spice netlist output. Extracted models fully capture inductance and resistance behavior from DC up to mm-wave frequencies. Extremely accurate, capturing all electromagnetic phenomena, including current distributions, skin and proximity effects.



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